

=> D HIS

(FILE 'HOME' ENTERED AT 08:06:01 ON 22 APR 2002)

FILE 'USPATFULL, USPAT2, INSPEC, EUROPATFULL' ENTERED AT 08:06:22 ON 22 APR 2002

L1 10867 S SYSTEM AND BEHAVIORAL
L2 80 S L1 AND IMPLEMENTABLE
L3 60 S L2 AND SIMULAT?
L4 46 S L3 AND SYNTHESIZ?
L5 46 S L4 AND DESCRIPTION
L6 0 S L5 AND IMPLMENTABLE DESCRIPTION
L7 46 S L5 AND DESIGN
L8 43 S L5 AND MODEL?
L9 41 S L8 AND OBJECT#
L10 25 S L9 AND IMPLEMENTABLE DESCRIPTION
L11 25 S L10 AND BEHAVIORAL DESCRIPTION
L12 2 S L11 AND SYNTHESIZABLE DESCRIPTION

=> D L12 1-2 IBIB ABS

L12 ANSWER 1 OF 2 USPATFULL

ACCESSION NUMBER: 2001:72770 USPATFULL

TITLE: Design environment and a method for generating an
implementable description of a
digital system

INVENTOR(S): Schaumont, Patrick, Wijgmaal, Belgium
Vernalde, Serge, Heverlee, Belgium
Cockx, Johan, Pellenberg, Belgium

PATENT ASSIGNEE(S): Interuniversitair Micro-Elektronica Centrum, Leuven,
Belgium (non-U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 6233540	B1	20010515
APPLICATION INFO.:	US 1998-41985		19980313 (9)

	NUMBER	DATE
PRIORITY INFORMATION:	US 1997-39078P	19970314 (60)
	US 1997-39079P	19970314 (60)
	US 1997-41121P	19970320 (60)
DOCUMENT TYPE:	Utility	
FILE SEGMENT:	Granted	
PRIMARY EXAMINER:	Teska, Kevin J.	
ASSISTANT EXAMINER:	Sergent, Douglas W.	
LEGAL REPRESENTATIVE:	Knobbe, Martens, Olson & Bear, LLP	
NUMBER OF CLAIMS:	27	
EXEMPLARY CLAIM:	1	
NUMBER OF DRAWINGS:	23 Drawing Figure(s); 21 Drawing Page(s)	
LINE COUNT:	1739	

AB The present invention is a design apparatus compiled on a computer environment for generating from a **behavioral description of a system** comprising at least one digital system part, an **implementable description** for said system, said behavioral

description being represented on said computer environment as a first set of objects with a first set of relations therebetween, and implementable description represented on said computer environment as a second set of objects with a second set of relations therebetween, said first and second set of objects being part of a design environment.

L12 ANSWER 2 OF 2 EUROPATFULL COPYRIGHT 2002 WILA

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

ACCESSION NUMBER: 867820 EUROPATFULL EW 199840 FS OS
 TITLE: A design environment and a method for generating an implementable description of a digital system.
 Eine Entwurfsumgebung und Verfahren zum Erzeugen einer realisierbaren Beschreibung eines digitalen Systems.
 Environnement de conception et methode pour generer une description realisable d'un systeme digital.
 INVENTOR(S): Schaumont, Patrick, Nieuwstraat 16, 3018 Wijnmaal, BE;
 Vernalde, Serge, Celestijnenlaan 13/11, 3001 Heverlee, BE;
 Cox, Johan, Rijkweg 153, 3020 Herent, BE
 PATENT ASSIGNEE(S): INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW,
 Kapeldreef 75, 3001 Heverlee, BE
 PATENT ASSIGNEE NO: 1021504
 AGENT: Van Malderen, Joelle et al, Office Van Malderen, Place Reine Fabiola 6/1, 1083 Bruxelles, BE
 AGENT NUMBER: 75971
 OTHER SOURCE: ESP1998067 EP 0867820 A2 980930
 SOURCE: Wila-EPZ-1998-H40-T2a
 DOCUMENT TYPE: Patent
 LANGUAGE: Anmeldung in Englisch; Veroeffentlichung in Englisch
 DESIGNATED STATES: R AT; R BE; R CH; R DE; R DK; R ES; R FI; R FR; R GB; R GR; R IE; R IT; R LI; R LU; R MC; R NL; R PT; R SE
 PATENT INFO.PUB.TYPE: EPA2 EUROPAEISCHE PATENTANMELDUNG
 PATENT INFORMATION:

	PATENT NO	KIND DATE
	EP 867820	A2 19980930
'OFFENLEGUNGS' DATE:		19980930
APPLICATION INFO.:	EP 1998-870052	19980313
PRIORITY APPLN. INFO.:	US 1997-39079	19970314
	US 1997-41121	19970320

=> D HIS

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FILE 'USPATFULL, USPAT2, INSPEC, EUROPATFULL' ENTERED AT 08:06:22 ON 22 APR 2002

L1 10867 S SYSTEM AND BEHAVIORAL
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 L5 46 S L4 AND DESCRIPTION
 L6 0 S L5 AND IMPLMENTABLE DESCRIPTION
 L7 46 S L5 AND DESIGN
 L8 43 S L5 AND MODEL?
 L9 41 S L8 AND OBJECT#
 L10 25 S L9 AND IMPLEMENTABLE DESCRIPTION

=> D L11 1-25 IBIB ABS

L11 ANSWER 1 OF 25 USPATFULL

ACCESSION NUMBER: 2001:216451 USPATFULL

TITLE: Method and **system** for creating and validating low level **description** of electronic design

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
 Deeley, Richard, San Jose, CA, United States
 Nagasamy, Vijay, Union City, CA, United States
 Vafai, Manoucher, Los Gatos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
 (U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 6324678	B1	20011127
APPLICATION INFO.:	US 1996-701727		19960822 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1993-77403, filed on 14 Jun 1993, now patented, Pat. No. US 5553002		
	Continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993, now patented, Pat. No. US 5544067		
	Continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned Continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030		
	Continuation-in-part of Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512		
	Continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned		

DOCUMENT TYPE: Utility
 FILE SEGMENT: GRANTED
 PRIMARY EXAMINER: Trans, Vincent N.
 ASSISTANT EXAMINER: Jones, Hugh
 NUMBER OF CLAIMS: 23
 EXEMPLARY CLAIM: 1
 NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
 LINE COUNT: 3064

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. A matrix of

milestones (goals in the design activity) is defined by degree of complexity (level of abstraction) of a design and for progressive stages (levels) of design activity (from concept through implementation). The milestones are defined using continuous refinement, and the design activity proceeds towards subsequent milestones. As milestones are achieved, previous design activity becomes unalterable. A feasibility stage is key to convergence of the process. Single level or multi-level estimators determine the direction of the process.

L11 ANSWER 2 OF 25 USPATFULL

ACCESSION NUMBER: 2001:72770 USPATFULL

TITLE: Design environment and a method for generating an implementable description of a digital system

INVENTOR(S): Schaumont, Patrick, Wijgmaal, Belgium
Vernalde, Serge, Heverlee, Belgium
Cockx, Johan, Pellenberg, Belgium

PATENT ASSIGNEE(S): Interuniversitair Micro-Elektronica Centrum, Leuven, Belgium (non-U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 6233540	B1	20010515
APPLICATION INFO.:	US 1998-41985		19980313 (9)

	NUMBER	DATE
PRIORITY INFORMATION:	US 1997-39078P	19970314 (60)
	US 1997-39079P	19970314 (60)
	US 1997-41121P	19970320 (60)
DOCUMENT TYPE:	Utility	
FILE SEGMENT:	Granted	
PRIMARY EXAMINER:	Teska, Kevin J.	
ASSISTANT EXAMINER:	Sergeant, Douglas W.	
LEGAL REPRESENTATIVE:	Knobbe, Martens, Olson & Bear, LLP	
NUMBER OF CLAIMS:	27	
EXEMPLARY CLAIM:	1	
NUMBER OF DRAWINGS:	23 Drawing Figure(s); 21 Drawing Page(s)	
LINE COUNT:	1739	

AB The present invention is a design apparatus compiled on a computer environment for generating from a **behavioral description** of a **system** comprising at least one digital **system** part, an **implementable description** for said **system**, said **behavioral description** being represented on said computer environment as a first set of **objects** with a first set of relations therebetween, said **implementable description** being represented on said computer environment as a second set of **objects** with a second set of relations therebetween, said first and second set of **objects** being part of a design environment.

L11 ANSWER 3 OF 25 USPATFULL

ACCESSION NUMBER: 2001:53471 USPATFULL

TITLE: Method and **system** for creating, validating, and scaling structural **description** of electronic device

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Mintz, Doron, Sunnyvale, CA, United States
Vafai, Manouchshir, Los Gatos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States (U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 6216252	B1	20010
APPLICATION INFO.:	US 1996-701236		19960822 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1994-193306, filed on 8 Feb		

5544066

1994 Continuation-in-part of Ser. No. US 1993-76729, filed on 14 Jun 1993, now patented, Pat. No. US

Continuation-in-part of Ser. No. US 1993-76738, filed on 14 Jun 1993, now patented, Pat. No. US 5557531
Continuation-in-part of Ser. No. US 1993-76728, filed on 14 Jun 1993, now patented, Pat. No. US 5541849
Continuation-in-part of Ser. No. US 1993-77403, filed on 14 Jun 1993, now patented, Pat. No. US 5553002 , said Ser. No. US 76729 Continuation-in-part of Ser.

No.

US 1993-54053, filed on 26 Apr 1993, now abandoned , said Ser. No. US 76738 Continuation-in-part of Ser.

No.

US 54053 , said Ser. No. US 76728 Continuation-in-part of Ser. No. US 54053 , said Ser. No. US 77403
Continuation-in-part of Ser. No. US 54053
Continuation-in-part of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030 ,

said

Ser. No. US 76729 Continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993, now patented, Pat. No. US 5544067 , said Ser. No. US 76738
Continuation-in-part of Ser. No. US 77294 , said Ser. No. US 76728 Continuation-in-part of Ser. No. US 77294 , said Ser. No. US 77403 Continuation-in-part of Ser. No. US 77294 Continuation-in-part of Ser. No. US 54053
Continuation-in-part of Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512
Continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Teska, Kevin J.
ASSISTANT EXAMINER: Jones, Hugh
NUMBER OF CLAIMS: 21
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 23 Drawing Figure(s); 21 Drawing Page(s)
LINE COUNT: 3454

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic technique

to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels

of design representations. At each level, the intended meaning and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; high level what-if analysis; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators for partitioning and evaluating a design prior to logic synthesis. From the structural **description** , a physical implementation of the device is readily realized.

Techniques for scaling of a model design to provide a scaled design are described whereby parameters of a model design such as size, circuit complexity, interconnection complexity, number of I/O connections, etc., can be scaled to produce a scaled version of the design. The scaling techniques employ multi-level hierarchical module replication to produce fully-functional scaled designs which closely match the function of the model design. Test vectors for the scaled designs can be readily obtained by altering test vectors for the model design to account for the replicated modules.

L11 ANSWER 4 OF 25 USPATFULL

ACCESSION NUMBER: 1999:89930 USPATFULL

TITLE: Method and system for creating and verifying structural logic model of electronic design from behavioral description, including generation of logic and timing models

INVENTOR(S): Rostoker, Michael D., Boulder Creek, CA, United States
Dangelo, Carlos, Los Gatos, CA, United States
Bair, Owen S., Saratoga, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States (U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5933356		19990803
APPLICATION INFO.:	US 1996-740967		19961105 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1994-246798, filed on 20 May 1994, now patented, Pat. No. US 5572437 which is a continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993, now patented, Pat. No. US 5544067 Ser. No. Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned And Ser. No. US 1993-85658, filed on 30 Jun 1993, now patented, Pat. No. US 5463563 which is a continuation of Ser. No. US 1991-684668, filed on 12 Apr 1991, now patented, Pat. No. US 5278769, said		
Ser.	No. US 54053 which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030		
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		
NUMBER OF CLAIMS:	13		
EXEMPLARY CLAIM:	1		
NUMBER OF DRAWINGS:	28 Drawing Figure(s); 25 Drawing Page(s)		
LINE COUNT:	1976		

AB A system and method are provided herein for creating and validating an electronic design structural description of a circuit or device from a VHDL description of the circuit or device which includes a compiler for compiling the VHDL description of the circuit or device; a device for locating problems within the compiled description and measuring the effectiveness of solving the problems; a device for passing information including the compiled description to a physical design level; a physical design tool for receiving the information and creating a physical design therefrom; and a device for back annotating the information from the physical design tool to the compiler.

L11 ANSWER 5 OF 25 USPATFULL

ACCESSION NUMBER: 1999:65650 USPATFULL

TITLE: Specification and design of complex digital systems

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States

PATENT ASSIGNEE(S):

Nagasamy, Vijay, Union City, CA, United States
LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5910897		19990608
APPLICATION INFO.:	US 1997-890174		19970709 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1996-603037, filed on 16 Feb 1996, now abandoned which is a continuation of Ser.		
	No. US 1994-252231, filed on 1 Jun 1994, now patented, Pat. No. US 5493508		
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		
NUMBER OF CLAIMS:	20		
EXEMPLARY CLAIM:	1		
NUMBER OF DRAWINGS:	18 Drawing Figure(s); 15 Drawing Page(s)		
LINE COUNT:	1834		
AB	A methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions . The design activity is essentially a series of transformations operating upon various levels of design representations. At each level the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, descriptions , constraints and trade-offs; architectural partitioning; what-if analysis at a-high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural description , a physical implementation of the device is readily realized. The methodology further includes an automated interactive, iterative technique for creating a system -level specification in a directly-executable formal specification language. This technique makes use of formal verification and feasibility analysis techniques to iteratively refine the specification prior to implementation. This iterative refinement eliminates many ambiguities and inconsistencies from the specification, and ensures that there is at least one realizable implementation of the specification. The formal verification techniques are further employed to ensure that as the design progresses, compliance with the specification is maintained, and that any specification change is reflected and accounted for, both system -wide and implementation-wide.		

L11 ANSWER 6 OF 25 USPATFULL

ACCESSION NUMBER: 1999:31642 USPATFULL
TITLE: Methodology for deriving executable low-level structural **descriptions** and valid physical implementations of circuits and **systems** from semantic specifications and **descriptions** thereof
INVENTOR(S): Dangelo, Carlos, San Jose, CA, United States

States

Nagasamy, Vijay Kumar, Mountain View, CA, United

Bootehsaz, Ahsan, Santa Clara, CA, United States

Rajan, Sreeranga Prasannakumar, Sunnyvale, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5880971		19990309
APPLICATION INFO.:	US 1997-905917		19970804 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1996-607434, filed on 28 Feb 1996, now abandoned which is a continuation of		
Ser.	No. US 1994-355105, filed on 13 Dec 1994, now		
patented,	Pat. No. US 5536277 which is a continuation of Ser.		
No.	US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030		
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		
NUMBER OF CLAIMS:	58		
EXEMPLARY CLAIM:	1		
NUMBER OF DRAWINGS:	15 Drawing Figure(s); 13 Drawing Page(s)		
LINE COUNT:	1408		
AB	A methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications is disclosed. The methodology uses a systematic technique		
levels	to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions . The design activity is essentially a series of transformations operating upon various		
of design representations.	At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals.		
Important features of the methodology are:	capturing the users		
concepts,	intent, specification, descriptions , constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure.		
a	The methodology includes using estimators, based on data gathered over		
	number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural description , a physical implementation of the device is readily realized.		

L11 ANSWER 7 OF 25 USPATFULL

ACCESSION NUMBER: 1999:19955 USPATFULL

TITLE: Method and **system** for creating and validating low-level **description** of electronic design

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Nagasamy, Vijay, Union City, CA, United States
Ponukumati, Vijayanand, Sunnyvale, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

NUMBER	KIND	DATE
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PATENT INFORMATION: US 5870308 19990209
APPLICATION INFO.: US 1996-742359 1996-742359 (8)
RELATED APPLN. INFO: Continuation of Ser. No. US 1996-742359, filed on 2 Jun

1994, now patented, Pat. No. US 5572436 which is a continuation-in-part of Ser. No. US 1993-76729, filed on 14 Jun 1993, now patented, Pat. No. US 5544066 Ser. No. Ser. No. US 1993-76738, filed on 14 Jun 1993, now patented, Pat. No. US 5557531 Ser. No. Ser. No. US 1993-76728, filed on 14 Jun 1993, now patented, Pat. No. US 5541849 And Ser. No. US 1993-77403, filed on 14 Jun 1993, now patented, Pat. No. US 5553002, said

Ser.

No. US 20 -76729 Ser. No. Ser. No. US 20 -76738 Ser. No. Ser. No. US 20 -76728 And Ser. No. US 20 -77403

each Ser. No. US 20 - which is a continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned And Ser. No. US 20 -77294 which is a continuation-in-part of Ser. No. US 20 -54053 And

Ser.

No. US 1992-917801, filed on 20 Jul 1992, now

patented,

Pat. No. US 5220512 which is a continuation of Ser.

No.

US 1990-512129, filed on 19 Apr 1990, now abandoned, said Ser. No. US 20 -54053 which is a continuation of Ser. No. US 1990-507201, filed on 19 Apr 1990, now patented, Pat. No. US 5222030

DOCUMENT TYPE:

Utility

FILE SEGMENT:

Granted

PRIMARY EXAMINER:

Teska, Kevin J.

ASSISTANT EXAMINER:

Kik, Phallaka

NUMBER OF CLAIMS:

37

EXEMPLARY CLAIM:

1

NUMBER OF DRAWINGS:

21 Drawing Figure(s); 19 Drawing Page(s)

LINE COUNT:

3348

AB

A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic

technique

to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various

levels

of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals.

Important features of the methodology are: capturing the users concepts,

intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over

a

number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. Techniques are described for estimating ancillary parameters of the device (such

as

device cost, production speed, production lead time, etc.), at early, high level stages of the design process (e.g., at the **system**, **behavioral**, and register transfer level stages). The techniques can be applied to optimize the design characteristics other than

measurable physical characteristics, such as those deriving from
project time and cost constraints.

L11 ANSWER 8 OF 25 USPATFULL

ACCESSION NUMBER: 1999:16735 USPATFULL

TITLE: **System** and method for creating and validating
structural **description** of electronic
system from higher-level and behavior-oriented
description

INVENTOR(S): Rostoker, Michael D., San Jose, CA, United States
Watkins, Daniel R., Los Altos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5867399		19990202
APPLICATION INFO.:	US 1997-847930		19970421 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1993-77304, filed on 14 Jun 1993, now patented, Pat. No. US 5623418 which is a continuation-in-part of Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512, issued on 15 Jun 1993 And Ser. No. US 1993-77294, filed on 14 Jun 1993, now patented, Pat. No. US 5544067 which is a continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030, issued on 22 Jun 1993		
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		
NUMBER OF CLAIMS:	19		
EXEMPLARY CLAIM:	1		
NUMBER OF DRAWINGS:	49 Drawing Figure(s); 37 Drawing Page(s)		
LINE COUNT:	3060		
AB	A system for interactive design and simulation of an electronic circuit allowing a user to design a circuit by graphical entry and to view full or partial simulation and design results simultaneously, on a single display window. The user is able to define the form of a display of speed, delay, loading, symbols, simulation input and/or output values on each node and any path of the design. Simulation may be user-defined or other process time. The user is further able to view any information relevant to any object in the design at any level of design abstraction, and is able to view multiple levels of design abstraction simultaneously and to display information common to the various representations.		

L11 ANSWER 9 OF 25 USPATFULL

ACCESSION NUMBER: 1998:105517 USPATFULL

TITLE: Method and **system** for creating and validating
low level **description** of electronic design
from higher level, behavior-oriented
description, including interactive
system for hierarchical display of control and
dataflow information

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States

PATENT ASSIGNEE(S):

Watkins, Daniel, Los Altos, CA, United States
Mintz, Doron, Sunnyvale, CA, United States
LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5801958		19980901
APPLICATION INFO.:	US 1996-707918		19960910 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1994-196337, filed on 10 Feb 1994, now patented, Pat. No. US 5555201 which is a continuation-in-part of Ser. No. US 1993-77304, filed on 14 Jun 1993, now abandoned which is a continuation-in-part of Ser. No. US 1993-76729, filed on 14 Jun 1993, now patented, Pat. No. US 5544066		

which

is a continuation-in-part of Ser. No. US 1993-76738, filed on 14 Jun 1993, now patented, Pat. No. US

5557531

which is a continuation-in-part of Ser. No. US 1993-76728, filed on 14 Jun 1993, now patented, Pat. No. US 5541849 which is a continuation-in-part of Ser. No. US 1993-77403, filed on 14 Jun 1993, now patented, Pat. No. US 5553002

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Oppenheimer Wolff & Donnelly LLP
NUMBER OF CLAIMS: 40
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 65 Drawing Figure(s); 49 Drawing Page(s)
LINE COUNT: 5238

AB A technique for hierarchical display of control and dataflow graphs allowing a user to view hierarchically filtered control and dataflow information related to a design. The technique employs information inherent in the design **description** and information derived from design synthesis to identify "modules" of the design and design hierarchy. The user can specify a level of detail to be displayed for any design element or group of design elements. Any CDFG (control and dataflow graph) **object** can be "annotated" with a visual attribute or with text to indicate information about the design elements represented by the **object**. For example, block size, interior color, border color, line thickness, line style, etc., can be used to convey quantitative or qualitative information about a CDFG **object**. Examples of information which can be used to "annotate" **objects** include power dissipation, propagation delay, the number of HDL statement represented, circuit area, number of logic gates, etc. The user is able to expand and/or compress CDFG blocks either "in-place" on a higher level CDFG display or to be displayed in isolation. **Simulation**-related data can also be used to annotate the CDFG. By viewing CDFG's (particularly annotated CDFG's) for a variety of trial designs, a problem-solving user can gain quick insight into the effects and effectiveness of various design choices.

L11 ANSWER 10 OF 25 USPATFULL

ACCESSION NUMBER: 97:34211 USPATFULL

TITLE: **System** and method for creating and validating structural **description** of electronic **system**

INVENTOR(S): Rostoker, Michael D., San Jose, CA, United States
Watkins, Daniel R., Los Altos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5623418		19970422
APPLICATION INFO.:	US 1993-77304		19930614 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993 And Ser. No. US 1992-917801, filed on		

20

Jul 1992, now patented, Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned ,

said

Ser. No. US -77294 which is a continuation-in-part

of

Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030, issued on 22 Jun 1993

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 17
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 49 Drawing Figure(s); 37 Drawing Page(s)
LINE COUNT: 3242

AB A **system** for interactive design and **simulation** of an electronic circuit allowing a user to design a circuit by graphical entry and to view full or partial **simulation** and design results simultaneously, on a single display window. The user is able to define the form of a display of speed, delay, loading, symbols, **simulation** input and/or output values on each node and any path of the design. **Simulation** may be user-defined or other process time. The user is further able to view any information relevant to any **object** in the design at any level of design abstraction, and is able to view multiple levels of design abstraction simultaneously and to display information common to the various representations.

L11 ANSWER 11 OF 25 USPATFULL

ACCESSION NUMBER: 97:8441 USPATFULL

TITLE: Method and **system** for creating, validating, and scaling structural **description** of electronic device

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Mintz, Doron, Sunnyvale, CA, United States
Vafai, Manouchehr, Los Gatos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5598344		19970128
APPLICATION INFO.:	US 1994-193306		19940208 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-76729, filed on 14 Jun 1993, now patented, Pat. No. US 5544066 And Ser. No. US 1993-76738, filed on 14 Jun 1993, now patented, Pat. No. US 5557531 And Ser. No. US 1993-76728, filed on 14 Jun 1993, now patented, Pat. No. US 5541849 And Ser. No. US 1993-77403, filed on 14		

Ser.

Jun 1993, now patented, Pat. No. US 5553002 , each

No. US - which is a continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993 And Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No. US -54053 And Ser. No. US 1992-917801, filed on 20 Jul 1992, now

patented,

Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned , said Ser. No. US -54053 which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US

5222030,

issued on 22 Jun 1993

DOCUMENT TYPE:

Utility

FILE SEGMENT:

Granted

PRIMARY EXAMINER:

Trans, Vincent N.

LEGAL REPRESENTATIVE:

Poms, Smith, Lande & Rose

NUMBER OF CLAIMS:

19

EXEMPLARY CLAIM:

14

NUMBER OF DRAWINGS:

23 Drawing Figure(s); 20 Drawing Page(s)

LINE COUNT:

3510

AB

A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels

of

design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more

detailed

level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. Techniques for scaling of a **model** design to provide a scaled design are provided whereby parameters of a **model** design such as size, circuit complexity, interconnection density, number of I/O connections, etc., can be scaled to produce a scaled version of the design. The scaling techniques employ multi-level hierarchical module replication

to

produce fully-functional scaled designs which closely match the

function

of the **model** design. Test vectors for the scaled designs can be readily obtained by altering test vectors for the **model** design to account for the replicated modules.

L11 ANSWER 12 OF 25 USPATFULL

ACCESSION NUMBER:

96:102196 USPATFULL

TITLE:

Method and **system** for creating and verifying structural logic **model** of electronic design from **behavioral description**, including generation of logic and timing **models**

INVENTOR(S):

Rostoker, Michael D., Boulder Creek, CA, United States
Dangelo, Carlos, Los Gatos, CA, United States
Bair, Owen S., Sarotoga, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5572437		19961105
APPLICATION INFO.:	US 1994-246798		19940520 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-85658, filed on 30 Jun 1993 Ser. No. Ser. No. US 1993-54053, filed on 26 Apr 1993 And Ser. No. US 1993-77294, filed on 14 Jun 1993 , said Ser. No. US -85658 which is a continuation of Ser. No. US 1991-684668, filed on 12 Apr 1991, now patented, Pat. No. US 5278769 , said		
Ser.	No. US -54053 which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030		
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		
LEGAL REPRESENTATIVE:	Poms, Smith, Lande & Rose		
NUMBER OF CLAIMS:	17		
EXEMPLARY CLAIM:	1		
NUMBER OF DRAWINGS:	28 Drawing Figure(s); 25 Drawing Page(s)		
LINE COUNT:	2014		

AB An automatic logic-model generation system operates on a behavioral description of an electronic design (e.g., a circuit, a system, etc.) to automatically generate a low-level (i.e., circuit-level) design of the electronic design, to lay out the electronic design for production in the form of an integrated circuit, and to produce logic-level models incorporating accurate timing (and delay) information. A verification process is also performed whereby the logic-level model is automatically verified for accuracy.

L11 ANSWER 13 OF 25 USPATFULL

ACCESSION NUMBER: 96:102195 USPATFULL
TITLE: Method and system for creating and validating low level description of electronic design
INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Nagasamy, Vijay, Union City, CA, United States
Ponukumati, Vijayanand, Sunnyvale, CA, United States
PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5572436		19961105
APPLICATION INFO.:	US 1994-252823		19940602 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-76729, filed on 14 Jun 1993 Ser. No. Ser. No. US 1993-76738, filed on 14 Jun 1993 Ser. No. Ser. No. US 1993-76728, filed on 14 Jun 1993 And Ser. No. US 1993-77403, filed on 14 Jun 1993 , each Ser. No. US - which is a continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993 And Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No.		
US	-54053 And Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned , said Ser. No. US -54053		

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 19
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
LINE COUNT: 3315

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications using a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. Techniques are provided for estimating ancillary parameters of the device (such as device cost, production speed, production lead time, etc.), at early, high level stages of the design process (e.g., at the **system**, **behavioral**, and register transfer level stages). The techniques can be applied to optimize the design characteristics other than measurable physical characteristics, such as those deriving from project time and cost constraints.

L11 ANSWER 14 OF 25 USPATFULL

ACCESSION NUMBER: 96:85802 USPATFULL

TITLE: Method and **system** for creating and validating low level structural **description** of electronic design from higher level, behavior-oriented **description**, including estimating power dissipation of physical implementation

INVENTOR(S): Rostoker, Michael D., San Jose, CA, United States
Dangelo, Carlos, Los Gatos, CA, United States
Nagasamy, Vijay, Union City, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5557531		19960917
APPLICATION INFO.:	US 1993-76738		19930614 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512, issued on 15 Jun 1993 And Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030,		

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 35
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
LINE COUNT: 3252

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized.

Techniques are described for estimating the power and area requirements of the physical implementation of the device, at early, high level stages of the design process (e.g., at the **system**, **behavioral**, and register transfer level stages). The techniques are suited to the design of any semiconductor device, particularly CMOS devices.

L11 ANSWER 15 OF 25 USPATFULL

ACCESSION NUMBER: 96:83270 USPATFULL

TITLE: Method and **system** for creating and validating low level **description** of electronic design from higher level, behavior-oriented **description**, including interactive **system** for hierarchical display of control and dataflow information

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Watkins, Daniel, Los Altos, CA, United States
Mintz, Doron, Sunnyvale, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5555201		19960910
APPLICATION INFO.:	US 1994-196337		19940210 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-77304, filed on 14 Jun 1993 Ser. No. Ser. No. US 1993-76729, filed on 14 Jun 1993 Ser. No. Ser. No. US 1993-76738, filed on 14 Jun 1993 Ser. No. Ser. No. US 1993-76728, filed		

of

patented,

DOCUMENT TYPE:

FILE SEGMENT:

PRIMARY EXAMINER:

LEGAL REPRESENTATIVE:

NUMBER OF CLAIMS:

EXEMPLARY CLAIM:

NUMBER OF DRAWINGS:

LINE COUNT:

AB

A technique for hierarchical display of control and dataflow graphs allowing a user to view hierarchically filtered control and dataflow information related to a design. The technique employs information inherent in the design **description** and information derived from design synthesis to identify "modules" of the design and design hierarchy. The user can specify a level of detail to be displayed for any design element or group of design elements. Any CDFG (control and dataflow graph) **object** can be "annotated" with a visual attribute or with text to indicate information about the design elements represented by the **object**. For example, block size, interior color, border color, line thickness, line style, etc., can be used to convey quantitative or qualitative information about a CDFG **object**. Examples of information which can be used to "annotate" **objects** include power dissipation, propagation delay, the number of HDL statement represented, circuit area, number of logic gates, etc. The user is able to expand and/or compress CDFG blocks either "in-place" on a higher level CDFG display or to be displayed in isolation. **Simulation**-related data can also be used to annotate the CDFG. By viewing CDFG's (particularly annotated CDFG's) for a variety of trial designs, a problem-solving user can gain quick insight into the effects and effectiveness of various design choices.

L11 ANSWER 16 OF 25 USPATFULL

ACCESSION NUMBER: 96:80864 USPATFULL

TITLE: Method and **system** for creating and validating low level **description** of electronic design from higher level, behavior-oriented **description**, using milestone matrix incorporated into user-interface

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Deeley, Richard, San Jose, CA, United States
Nagasamy, Vijay, Union City, CA, United States
Vafai, Manoucher, Los Gatos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

NUMBER KIND DATE

PATENT INFORMATION: US 5553002 19960903
APPLICATION INFO.: US 1993-77403 1993 (8)
DISCLAIMER DATE: 20100622
RELATED APPLN. INFO.: Continuation-in-part of Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993 which is a continuation of Ser. No. US 1990-507201, filed on 6

Apr

1990, now patented, Pat. No. US 5222030, issued on 22 Jun 1993, said Ser. No. US -77294 which is a continuation-in-part of Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now

abandoned

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 23
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
LINE COUNT: 3243

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications using a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. A top-down design methodology is described, wherein a matrix of milestones (goals in the design activity) is defined by degree of complexity (level of abstraction) of a design and for progressive stages (levels) of design activity (from concept through implementation). The milestones are defined in a monotonic, unidirectional manner using continuous refinement, and the design activity proceeds towards subsequent milestones. As milestones are achieved, previous design activity

becomes

fixed and unalterable. A feasibility stage is key to convergence of the process. Single level or multi-level estimators (predictors) determine the direction of the process.

L11 ANSWER 17 OF 25 USPATFULL

ACCESSION NUMBER: 96:71099 USPATFULL

TITLE: Method and **system** for creating, deriving and validating structural **description** of electronic **system** from higher level, behavior-oriented **description**, including interactive schematic design and **simulation**

INVENTOR(S): Rostoker, Michael D., Boulder Creek, CA, United States
Dangelo, Carlos, Los Gatos, CA, United States
Watkins, Daniel R., Los Altos, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5544067		19960806
APPLICATION INFO.:	US 1993-77294		19930614 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned And Ser. No. US 1992-917801, filed on 20 Jul 1992, now patented, Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned, said Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6		

Apr

1990, now patented, Pat. No. US 5222030, issued on 22 Jun 1993

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 31
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 26 Drawing Figure(s); 21 Drawing Page(s)
LINE COUNT: 2427

AB A **system** for interactive design, synthesis and **simulation** of an electronic **system** allowing a user to design a **system** either by specification of a **behavioral model** in a high level language such as VHDL or by graphical entry. The user can view full or partial **simulation** and design results simultaneously, on a single display window. The synthesis process uses a systematic technique to

map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is generally a series of transformations operating upon various levels of design representations. At each level, the design can be **simulated** and reviewed in schematic diagram form. The **simulation** results can be displayed immediately adjacent to signal lines on the diagram to which they correspond. In one embodiment,

design rule violations are processed by an expert **system** to suggest possible corrections or alterations to the design which will eliminate the design rule violations. Schematic diagram and **simulation** displays showing those portions of the electronic **system** and **simulated** signal patterns which are related to the design rule violations are used to help the user identify and appropriately correct problems in the design.

L11 ANSWER 18 OF 25 USPATFULL

ACCESSION NUMBER: 96:71098 USPATFULL

TITLE: Method and **system** for creating and validating low level **description** of electronic design from higher level, behavior-oriented **description**, including estimation and

comparison of low-level design constraints

INVENTOR(S): Rostoker, Michael D., San Jose, CA, United States
Dangelo, Carlos, Los Gatos, CA, United States
Nagasamy, Vijay, Union City, CA, United States
Mintz, Doron, Sunnyvale, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5544066		1996
APPLICATION INFO.:	US 1993-76729		19930614 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned And Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No. US -54053 And Ser. No. US 1992-917801, filed on 20 Jul 1992, now		

patented,

Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned, said Ser. No. US -54053 which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US

5222030,

issued on 22 Jun 1993

DOCUMENT TYPE: Utility
 FILE SEGMENT: Granted
 PRIMARY EXAMINER: Trans, Vincent N.
 LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
 NUMBER OF CLAIMS: 24
 EXEMPLARY CLAIM: 1
 NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
 LINE COUNT: 3235

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications using a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. Techniques are provided for constraint-driven partitioning of **behavioral descriptions**, and effective partitioning of high level **descriptions** for synthesis of multiple chips or blocks at the logic or register transfer levels. The partitioning technique is level-independent, and is integrated with the top-down design process, and takes into account constraints such as area, timing, power, package cost and testability. Iterative refinement is used to arrive at partitions that meet constraints imposed at high levels of abstraction.

L11 ANSWER 19 OF 25 USPATFULL

ACCESSION NUMBER: 96:68662 USPATFULL

TITLE: Method and **system** for creating and validating low level **description** of electronic design from higher level, behavior-oriented **description**, including estimation and comparison of timing parameters

INVENTOR(S): Rostoker, Michael D., Boulder Creek, CA, United States
 Dangelo, Carlos, Los Gatos, CA, United States
 Mintz, Doron, Sunnyvale, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5541849		19960730
APPLICATION INFO.:	US 1993-76728		19930614 (8)
DISCLAIMER DATE:	20100622		
RELATED APPLN. INFO.:	Continuation-in-part of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned And Ser. No. US 1993-77294, filed on 14 Jun 1993 which is a continuation-in-part of Ser. No. US -54053 And Ser. No. US 1992-917801, filed on 20 Jul 1992, now		

patented,

Pat. No. US 5220512, issued on 15 Jun 1993 which is a continuation of Ser. No. US 1990-512129, filed on 19 Apr 1990, now abandoned, said Ser. No. US -54053 which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US

5222030,

issued on 22 Jun 1993

DOCUMENT TYPE: Utility
 FILE SEGMENT: Granted
 PRIMARY EXAMINER: Trans, Vincent N.
 LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
 NUMBER OF CLAIMS: 8
 EXEMPLARY CLAIM: 1
 NUMBER OF DRAWINGS: 20 Drawing Figure(s); 18 Drawing Page(s)
 LINE COUNT: 3126

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels

of

design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more

detailed

level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. Techniques are provided for estimating design performance, from **behavioral** /functional **descriptions**. Given a **behavioral** or a block diagram **description** of data flow in a design, pin-to-pin timing and minimum clock cycle for the design can be estimated accurately. An RTL **description** may thus be **synthesized** from a **behavioral description** such that timing constraints imposed at the **behavioral** level are achieved. The timing of a **synthesized** design is estimated, and the design is re-**synthesized** until a design is arrived at that meets timing constraints imposed at a higher level.

L11 ANSWER 20 OF 25 USPATFULL

ACCESSION NUMBER: 96:51566 USPATFULL

TITLE: ECAD **system** for deriving executable low-level structural **descriptions** and valid physical implementations of circuits and **systems** from

INVENTOR(S):

high-level semantic **descriptions** thereof
Dangelo, Carlos, San Jose, CA, United States
Nagasamy, Vijay K., Mountain View, CA, United States
Bootehsaz, Ahsan, Santa Clara, CA, United States
Rajan, Sreeranga P., Sunnyvale, CA, United States
PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5526277		19960611
APPLICATION INFO.:	US 1994-355105		19941213 (8)
RELATED APPLN. INFO.:	Continuation of Ser. No. US 1993-54053, filed on 26 Apr 1993, now abandoned which is a continuation of Ser. No. US 1990-507201, filed on 6 Apr 1990, now patented, Pat. No. US 5222030		

DOCUMENT TYPE: Utility
FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 24
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 21 Drawing Figure(s); 16 Drawing Page(s)
LINE COUNT: 1588

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized.

L11 ANSWER 21 OF 25 USPATFULL

ACCESSION NUMBER: 96:15399 USPATFULL

TITLE: Specification and design of complex digital systems

INVENTOR(S): Dangelo, Carlos, Los Gatos, CA, United States
Nagasamy, Vijay, Union City, CA, United States

PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5493508		19960220
APPLICATION INFO.:	US 1994-252231		19940601 (8)
DOCUMENT TYPE:	Utility		

FILE SEGMENT: Granted
PRIMARY EXAMINER: Trans, Vincent N.
LEGAL REPRESENTATIVE: Poms, Smith, Lande & Rose
NUMBER OF CLAIMS: 4
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 18 Drawing Figure(s); 15 Drawing Page(s)
LINE COUNT: 1701

AB A methodology for generating structural **descriptions** of complex digital devices from high-level **descriptions** and specifications is disclosed. The methodology uses a systematic technique

to map and enforce consistency of the semantics imbedded in the intent of the original, high-level **descriptions**. The design activity is essentially a series of transformations operating upon various

levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals.

Important features of the methodology are: capturing the users concepts,

intent, specification, **descriptions**, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over

a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural **description**, a physical implementation of the device is readily realized. The methodology further includes an automated interactive, iterative technique for creating a **system**-level specification in a directly-executable formal specification language. This technique makes use of formal verification and feasibility analysis techniques to iteratively refine the specification prior to implementation. This iterative refinement eliminates many ambiguities and inconsistencies from the specification, and ensures that there is at least one realizable implementation of the specification. The formal verification techniques are further employed to ensure that as the design

progresses,

compliance with the specification is maintained, and that any specification change is reflected and accounted for, both **system**-wide and implementation-wide.

L11 ANSWER 22 OF 25 USPATFULL

ACCESSION NUMBER: 93:50899 USPATFULL

TITLE: Methodology for deriving executable low-level structural **descriptions** and valid physical implementations of circuits and **systems** from high-level semantic specifications and **descriptions** thereof

INVENTOR(S): Dangelo, Carlos, San Jose, CA, United States
Nagasamy, Vijay K., Mountain View, CA, United States
Bootehsaz, Ahsan, Santa Clara, CA, United States
Rajan, Sreeranga P., Sunnyvale, CA, United States
PATENT ASSIGNEE(S): LSI Logic Corporation, Milpitas, CA, United States
(U.S. corporation)

	NUMBER	KIND	DATE
PATENT INFORMATION:	US 5222030		19930622
APPLICATION INFO.:	US 1990-507201		19900406 (7)
DOCUMENT TYPE:	Utility		
FILE SEGMENT:	Granted		
PRIMARY EXAMINER:	Trans, Vincent N.		

LEGAL REPRESENTATIVE: Linden, Gerald E., Rostoker, Michael D.
NUMBER OF CLAIMS: 23
EXEMPLARY CLAIM: 1
NUMBER OF DRAWINGS: 15 Drawing Figure(s); 13 Drawing Page(s)
LINE COUNT: 1249

AB A methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications is disclosed. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Important features of the methodology are: capturing the users concepts, intent, specification, descriptions, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural description, a physical implementation of the device is readily realized.

L11 ANSWER 23 OF 25 EUROPATFULL COPYRIGHT 2002 WILA

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

ACCESSION NUMBER: 991000 EUROPATFULL EW 200014 FS OS
TITLE: Reuse of hardware components.
Wiederverwendung von Hardwarekomponenten.
Reutilisation de composants materiels.
INVENTOR(S): Schaumont, Patrick, Nieuwstraat 16, 3018 Wijnmaal, BE;
Cmar, Radim, Murgasa 28, 971 01 Prievizda, SK;
Vernalde, Serge, Celestijnenlaan 13/11, 3001 Heverlee, BE
PATENT ASSIGNEE(S): INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW,
Kapeldreef 75, 3001 Heverlee, BE
PATENT ASSIGNEE NO: 1021504
AGENT: Van Malderen, Joelle et al., Office Van Malderen, Place
Reine Fabiola 6/1, 1083 Bruxelles, BE
AGENT NUMBER: 75971
OTHER SOURCE: BEPA2000025 EP 0991000 A2 0031
SOURCE: Wila-EPZ-2000-H14-T2a
DOCUMENT TYPE: Patent
LANGUAGE: Anmeldung in Englisch; Veroeffentlichung in Englisch
DESIGNATED STATES: R AT; R BE; R CH; R CY; R DE; R DK; R ES; R FI; R FR; R GB; R GR; R IE; R IT; R LI; R LU; R MC; R NL; R PT; R SE; R AL; R LT; R LV; R MK; R RO; R SI
PATENT INFO.PUB.TYPE: EPA2 EUROPAEISCHE PATENTANMELDUNG
PATENT INFORMATION:

PATENT NO	KIND	DATE
EP 991000	A2	20000405
		20000405
APPLICATION INFO.:	EP 1999-870149	19990709
PRIORITY APPLN. INFO.:	EP 1998-870205	19980929
	US 1999-273089	19990319

L11 ANSWER 24 OF 25 EUROPATFULL COPYRIGHT 2002 WILA

ACCESSION NUMBER: 867820 EUROPATFULL EW 199840 FS OS
TITLE: A design environment and a method for generating an
implementable description of a digital
system.
Eine Entwurfsumgebung und Verfahren zum Erzeugen einer
realisierbaren Beschreibung eines digitalen
Systems.
Environnement de conception et methode pour generer une
description realisable d'un systeme digital.

INVENTOR(S): Schaumont, Patrick, Nieuwstraat 16, 3018 Wijnmaal, BE;
Vernalde, Serge, Celestijnenlaan 13/11, 3001 Heverlee,
BE;
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PATENT ASSIGNEE(S): INTERUNIVERSITAIR MICRO-ELEKTRONICA CENTRUM VZW,
Kapeldreef 75, 3001 Heverlee, BE

PATENT ASSIGNEE NO: 1021504

AGENT: Van Malderen, Joelle et al, Office Van Malderen, Place
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AGENT NUMBER: 75971

OTHER SOURCE: ESP1998067 EP 0867820 A2 980930

SOURCE: Wila-EPZ-1998-H40-T2a

DOCUMENT TYPE: Patent

LANGUAGE: Anmeldung in Englisch; Veroeffentlichung in Englisch

DESIGNATED STATES: R AT; R BE; R CH; R DE; R DK; R ES; R FI; R FR; R GB; R
GR; R IE; R IT; R LI; R LU; R MC; R NL; R PT; R SE

PATENT INFO.PUB.TYPE: EPA2 EUROPÄISCHE PATENTANMELDUNG

PATENT INFORMATION:

	PATENT NO	KIND DATE
	EP 867820	A2 19980930
'OFFENLEGUNGS' DATE:		19980930
APPLICATION INFO.:	EP 1998-870052	19980313
PRIORITY APPLN. INFO.:	US 1997-39079	19970314
	US 1997-41121	19970320

L11 ANSWER 25 OF 25 EUROPATFULL COPYRIGHT 2002 WILA

PATENT APPLICATION - PATENTANMELDUNG - DEMANDE DE BREVET

ACCESSION NUMBER: 463301 EUROPATFULL EW 199201 FS OS STA B
TITLE: Methodology for deriving executable low-level
structural

descriptions and valid physical implementations
of circuits and **systems** from high-level
semantic specifications and **descriptions**
thereof.
Verfahren zur Gewinnung von ausfuehrbaren niedrigen
strukturellen Beschreibungen und gueltige physische
Durchfuehrungen von Schaltungen sowie Systeme aus hohen
semantischen Spezifikationen mit deren Beschreibungen.
Methode pour l'obtention de **descriptions**
structurelles a bas niveau executables et realisations
physiques valables de circuits et systemes a partir de
specifications semantiques a haut niveau et leurs
descriptions.

INVENTOR(S): Dangelo, Carlos, 35522 McCoppin Park Ct., San Jose CA
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Nagasamy, Vijay Kumar, 302 Easy St., Mountain View CA
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Clara CA 95051, US;
Rajan, Sreeranga Prasannakumar, 3655 Pruneridge Avenue

PATENT ASSIGNEE(S): 169, Santa Clara, CA 95051, US
 LSI LOGIC CORPORATION, 1551 McCarthy Boulevard,
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 PATENT ASSIGNEE NO: 561302
 AGENT: Thiel, Christian et al, Patentanwaelte Herrmann,
 Trentepohl, Kirschner, Grosse, Bockhorni,
 Schaeferstrasse 18, W-4690 Herne 1, DE
 AGENT NUMBER: 57841
 OTHER SOURCE: ESP1992001 EP 0463301 A2 920102
 SOURCE: Wila-EPZ-1992-H01-T2
 DOCUMENT TYPE: Patent
 LANGUAGE: Anmeldung in Englisch; Veroeffentlichung in Englisch
 DESIGNATED STATES: R DE; R FR; R GB; R IT; R NL
 PATENT INFO.PUB.TYPE: EPA2 EUROPAEISCHE PATENTANMELDUNG
 PATENT INFORMATION:

	PATENT NO	KIND DATE
	EP 463301	A2 19920102
'OFFENLEGUNGS' DATE:		19920102
APPLICATION INFO.:	EP 1991-105400	19910405
PRIORITY APPLN. INFO.:	US 1990-507201	19900406